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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/756,443	JOO, SUK-HO	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/232,928.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-9** are pending in the application, which is a Divisional of Application No. 10/232,928 filed 08/30/2002, USP 6,717,196 is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/232,928, filed 08/30/2002.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on January 12, 2004. The references cited on the PTOL 1449 form have been considered.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a sacrificial layer in claim 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended.

The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan").

Regarding claim **1**, Fig. 4 of Prior Art (AAPA) discloses as set forth in Background of the Invention (BOI), page 2, line 32-page 3, line 19, a method of forming a ferroelectric memory device, comprises:

preparing a semiconductor substrate (10) comprising an interlayer dielectric layer (12) and a capacitor lower electrode contact (14) formed through the interlayer dielectric layer;

forming a cylindrical capacitor lower electrode (35) on the interlayer dielectric layer, thereby covering the contact;

conformally stacking a ferroelectric layer (41) by using a chemical vapor deposition (CVD) technique (BOI, page 3, lines 15-16) over substantially the entire surface of the semiconductor substrate including the capacitor lower electrode, and

forming a thick upper electrode (43) stacked over the entire surface of the semiconductor substrate.

However, Fig. 4 of Prior Art fails to teach of forming a capacitor upper electrode in the shape of a spacer surrounding the sidewall of the ferroelectric layer.

Fazan teaches that a process for fabricating a capacitor in a semiconductor integrated circuit comprises the steps of forming a capacitor upper electrode spacer (44) surrounding the sidewall of the ferroelectric layer (40) as storage node electrodes (Fig. 8, col. 7, lines 15-20).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the upper electrode of the structure of Fig. 4 of Prior Art to include a capacitor upper electrode spacer surrounding the sidewall of the ferroelectric layer, as taught by Fazan in order to form storage node electrodes and to allow storage capacitor formation at densities greater than that achievable by conventional photolithographic means (Fazan, col. 3, lines 28-30).

Regarding claim **5**, Fig. 4 of Prior Art (AAPA) discloses the claimed limitations except for the method as claimed in claim **1**, wherein the forming of the lower electrode further

comprises: sequentially stacking a lower electrode layer and a hard mask layer over substantially the entire surface of the semiconductor substrate; forming a hard mask pattern through photolithopaphy and etching processes with respect to the hard mask layer; and etching the lower electrode layer by using the hard mask pattern as an etch mask to form the lower electrode. Fazan teaches in Figs. 3-5 as set forth in column 5, line 3-column 6, line 31, that the forming of the lower electrode further comprises sequentially stacking a lower electrode layer (34, 35) and a hard mask layer (36) over substantially the entire surface of the semiconductor substrate (20); forming a hard mask pattern through photolithopaphy and etching processes with respect to the hard mask layer; and etching the lower electrode layer by using the hard mask pattern as an etch mask to form the lower electrode. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the lower electrode further comprises sequentially stacking a lower electrode layer and a hard mask layer over substantially the entire surface of the semiconductor substrate; forming a hard mask pattern through photolithopaphy and etching processes with respect to the hard mask layer; and etching the lower electrode layer by using the hard mask pattern as an etch mask to form the lower electrode, as taught by Fazan in order for having an enhanced capacitance useful for high-density DRAM applications (Fazan, col. 3, lines 19-21).

Claims **2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan"), and further in view of Ochiai (USP: 6,043,526).

Regarding claim **2**, Fig. 4 of Prior Art (AAPA) and Fazan disclose the claimed limitations except for the method as claimed in claim **1**, further comprises forming a plate line over a region of the semiconductor substrate where the upper electrode is formed, the plate line being in electrical contact with the upper electrode. Ochiai teaches in Fig. 3 that a plate line (29) is formed over a region of the semiconductor substrate (10) where the upper electrode (26) is formed, the plate line being in electrical contact with the upper electrode (col. 6, lines 1-24). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate a plate line formed over the upper electrode, as taught by Ochiai in order to provide connections or contacts for applying voltages to the upper electrode via the plate line (col. 6, lines 20-24).

Regarding claim **3**, Fig. 4 of Prior Art (AAPA) and Fazan disclose the claimed limitations as claimed in claim **2**, except for the method in which plural ones of such capacitors are arranged across the semiconductor substrate surface, aûer forming the upper electrode and before forming the plate line, further comprising: stacking an insulation layer over substantially the entire surface of the semiconductor substrate, to pmially fill gaps between the capacitors, the insulation layer exposing at least a part of the upper electrode. Ochiai discloses in Fig. 3 in which plural ones of such capacitors are arranged across the semiconductor substrate surface, after forming the upper electrode and before forming the plate line, further comprises stacking an insulation layer (27) over substantially the entire surface of the semiconductor substrate, to partially fill gaps between the capacitors, the insulation layer exposing at least a part of the upper electrode (col. 9, lines 28-30). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form stacking an insulation layer over substantially the entire surface

of the semiconductor substrate, to partially fill gaps between the capacitors, the insulation layer exposing at least a part of the upper electrode in order to insulate the capacitors to prevent short circuit.

Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan"), and in view of Ochiai (USP: 6,043,526), and further in view of Maejima et al. (USP: 6,100,201 hereinafter referred to as "Maejima").

Fig. 4 of Prior Art (AAPA), Fazan and Ochiai disclose the claimed limitations as claimed in claim **3**, except for wherein the recessing of the insulation layer is performed by an etching process; and the etching process uses an etch gas including at least one gas selected from a group consisting of CHF3, CF4, Ar, and N2 to make the insulation layer have etch selectivities with respect to the upper electrode and the ferroelectric layer. Maejima teaches that a method of defining a dielectric layer of a capacitor in a manufacturing a semiconductor device comprises the steps of selectively etching the dielectric layer by a reactive ion etching with a mixture gas comprising Ar and Cl2 so that the dielectric layer of the capacitor receives almost no substantive damage in the etching process (col. 19, lines 11-17). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use selectively etching the dielectric layer by a reactive ion etching with a mixture gas comprising Ar and Cl2, as taught by Maejima, in the etching process so that the dielectric layer of the capacitor receives almost no substantive damage in the etching process.

Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan"), and further in view of Lee et al. (US Pub. No. 2001/002395 hereinafter referred to as "Lee").

Fig. 4 of Prior Art (AAPA) and Fazan disclose the claimed limitations as claimed in claim **5**, except for the method further comprises stacking a conductive adhesive assistant layer before stacking the lower electrode layer, wherein the adhesive assistant layer is patterned together with the lower electrode layer. Lee teaches that in a real FRAM structure, an adhesive layer may be interposed between the SiO2 insulating layer and the lower electrode in order to improve the adhesive property of the lower electrode as set forth in [0023]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an adhesive layer may be interposed between the insulating layer and the lower electrode, as taught by Lee, in order to improve the adhesive property of the lower electrode.

Claim **7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan"), and further in view of Cho (USP: 6,355,521).

Fig. 4 of Prior Art (AAPA) and Fazan disclose the claimed limitations as claimed in claim **1**, except for the method wherein the forming of the lower electrode comprises: forming a sacrificial layer at the semiconductor substrate; forming a contact hole at the lower electrode region of the sacrificial layer; filling the contact hole with a conductive layer; and removing a remnant part of the sacrificial layer. Cho teaches in Figs. 1A-1E that a method of manufacturing

a capacitor in a semiconductor device comprises forming a sacrificial layer (16) at the semiconductor substrate (11) (Fig. 1C, col. 3, line 8); forming a contact hole (A) at the lower electrode region of the sacrificial layer (Fig. 1A, col. 2, lines 36-39); filling the contact hole with a conductive layer (13) (Fig. 1A, col. 2, lines 40-42); and removing a remnant part of the sacrificial layer (Fig. 1D, col. 3, lines 32-33). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a capacitor in a semiconductor device comprising forming a sacrificial layer at the semiconductor substrate; forming a contact hole at the lower electrode region of the sacrificial layer; filling the contact hole with a conductive layer; and removing a remnant part of the sacrificial layer, as taught by Cho in order to prevent leak current and improve the electric characteristic of the capacitor (col. 1, lines 61-62).

Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan"), and in view of Cho (USP: 6,355,521), and further in view of Basol et al. (US Pub. No. 2003/0032373 A1 hereinafter referred to as "Basol").

Fig. 4 of Prior Art (AAPA), Fazan and Cho disclose the claimed limitations as claimed in claim **7**, except for the method wherein the filling of the contact hole is performed by an electroplate technique. Basol discloses that the electroplate method is used for filling the trenches and vias in the insulating layer in a typical process as set forth in [0005]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to fill the contact hole using an electroplate technique, as taught by Basol since it is known in the art.

Claim **9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 4 of Prior Art, Applicant admitted prior art (AAPA), in view of Fazan et al. (USP: 5,940,676 hereinafter referred to as "Fazan"), and further in view of Moise et al. (USP: 6,534,809 hereinafter referred to as "Moise").

Fig. 4 of Prior Art (AAPA) and Fazan disclose the claimed limitations as claimed in claim **1**, except for the method wherein the anisotropical etching of the upper electrode layer uses an etch gas including oxygen and a combination gas composed of at least one gas selected from a group consisting of Cl2, BC13, HBr, and Ar, to make the upper electrode layer have an etch selectivity with respect to the ferroelectric layer. Moise teaches in Fig. 4e that the etchant used to etch top electrode layer (308 and 310) should include an oxygen-containing gas (such as O2), and additional gases, such as Ar, N2, Cl2, BCl3, CF4, SF6, or a combination thereof may be included to improve the etch selectivity (col. 24, lines 25-32). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the etchant used to etch top electrode layer including an oxygen-containing gas (such as O2), and additional gases, such as Ar, N2, Cl2, BCl3, CF4, SF6, or a combination thereof may be included, as taught by Moise in order to improve the etch selectivity.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

AH

June 18, 2004

Andy Huynh

Patent Examiner